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IME03-011

To: Commissioner for Patents
PO Box 1450
Alexandria, VA 22313-1450

From: Stephen B. Ackerman, Reg. No. 37,761
28 Davis Ave.
Poughkeepsie, N.Y. 12603

Subject :
SERIAL No.: 10/763,304
FILING DATE : 01 February 2004
APPLICANT: S. Mathew
TITLE : "SALICIDE PROCESS FOR METAL GATE CMOS DEVICES"
ART UNIT: 2823
EXAMINER: T.Q. Dang

APPEAL BRIEF

Dear Sir:

In response to the Final Rejection of the Claims 1 - 12, 14 - 28, and 31, dated April 03, 2007, for the identified Application for patent please accept this Appeal Brief. No oral hearing is requested.

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner of Patents and Trademarks, PO Box 1450 Alexandria VA 22313-1450, on January 17, 2008.

Signature _____ Date 1/17/08

Name Stephen B. Ackerman, Reg.#37,761

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The Commissioner of Patents and Trademarks is hereby authorized to charge the fee of $500.00 associated with this appeal brief to Deposit Account No. 19-0033, along with any additional extension fee required.

With Best Regards

Stephen B. Ackerman, Reg. No. 37,761

REAL PARTY INTEREST:

The real party in interest for this application is the assignee:

Agency for Science, Technology and Research
20 Biopolis Way, #07-01 Centros
Singapore 138668

RELATED APPEALS AND INTERFERENCES:

There are no related appeals or interferences for this Unite States patent application.

STATUS OF CLAIMS:

Claims 1 - 12, 14 - 28, and 31 are pending in the Patent Application and have been rejected. Claims 13, 29, and 30 have been cancelled. This appeal is to the rejection of Claims 1 - 12, 14 - 28, and 31. The Claims Appendix has Listing of the Claims in numerical sequence.

STATUS OF THE AMENDMENTS:

Amendments were filed to Claims 1, and 16, subsequent to the final rejection dated April 03, 2007. No amendments pending.

SUMMARY OF THE CLAIMED SUBJECT MATTER

Independent Claim 1 describes the fabrication of a metal oxide semiconductor field effect transistor (MOSFET) device, featuring a metal silicide region formed directly on an underlying conductive gate structure shown schematically in Figs. 1 - 8 of the drawings, and described in the Specification on page 5, line 6, to page 10, line 4. The formation of the metal silicide region directly overlying a conductive gate structure (item 3b in fig. 2, described in specification on page 6 line 18), is accomplished via deposition of an amorphous silicon layer (item 4a in fig.1, described in specification on page 6 line 7), directly on a conductive layer (item 3a in fig.1, described in specification on page 6 line 3), which in turn overlays a gate insulator layer; (item 2a in fig 1, described in specification on page 5 line 15). patterning to form an amorphous silicon shape (item 4b in fig 2, described in specification on page 6 line 20) and an underlying conductive gate structure (item 3b in fig. 2 described in specification on page 6 line 20). After formation of composite insulator spacers (item 7 and 8 in fig 4, described in specification in page 7 line 16 to page 8 line 3) on the sides of the amorphous silicon shape and conductive gate structure a metal layer (item 10a in fig 6, described in specification on page 8 line 14), is deposited followed by an anneal procedure resulting in a metal silicide region (item 10c in fig.7, described in specification on page 9 line 1), formed on the underlying conductive gate structure via total consumption of the metal layer and via total consumption of the amorphous silicon region. Non-reacted portions (items 10a, in fig. 7, described in specification on page 9 line 13) of the metal layer residing on the sides of the composite insulator spacers are selectively removed.

The essence of Independent Claim 1 is the formation of a metal silicide region directly on an underlying conductive gate structure via total consumption of a metal layer and of an amorphous silicon shape and without the use of a stop layer located between the amorphous silicon shape and the underlying conductive gate structure.

Dependent Claims 2, 3, and 4, described in the Specification on page 5, lines 12 - 15, describe an N channel, P channel or complimentary (CMOS) MOSFET device to which this process is applied to.

Dependent Claim 5 and 6, described in the Specification on page 5 line 17 to page 6, line 6, and shown schematically in Fig 1, describe the thickness and mode of deposition of a gate insulator layer.

Dependent Claim 7, described in the Specification on page 6 line 3 to page 6 line 6, and shown schematically in Fig. 1, describe the conductive layer material, thickness and mode of deposition.

Dependent Claim 8, described in the Specification on page 6 line 6 to page 6 line 11, and shown schematically in Fig. 1, describe the amorphous silicon layer, thickness and mode of deposition.

Dependent Claim 9, described in the Specification on page 6 line 16 to page 6 line 21, as well as shown schematically in Fig. 2, describe the definition of the materials and method used

for definition of a conductive gate structure.

Dependent Claim 10, described in the Specification on page 7 line 14 to page 8 line 3, as well as schematically shown in Fig. 4, describe the composite insulator components and their thickness.

Dependent Claim 11, described in the Specification on page 8 line 14 to page 8 line 17, as well as schematically in Fig. 6, describe specific metal layer as well as the thickness of said metal layers used for metal silicide formation.

Dependent Claim 12, the anneal procedure and conditions used to form the metal silicide region are described in the Specification on page 8 line 18 to page 9 line 12, as well as in Fig. 7.

Dependent Claim 13, had been previously cancelled.

Dependent Claim 14, described in the Specification on page 9 line 7 to page 9 line 8, as well as schematically using Fig. 7, describe the total consumption of the amorphous silicon layer during metal silicide formation.

Dependent Claim 15, described in the Specification on page 9 line 13 to page 9 line 21, and schematically in Fig. 8, the selective removal of non-reacted metal from the surfaces of the composite insulator spacers.

Independent Claim 16 describes the fabrication of a metal oxide semiconductor field effect

transistor (MOSFET) device, featuring a metal silicide region formed directly on an underlying conductive gate structure in turn overlying a high k gate insulator layer, shown schematically in Figs. 1 - 8 of the drawings, and described in the Specification on page 5, line 6, to page 10, line 4. The formation of the metal silicide region directly overlying a conductive gate structure is accomplished via deposition of an amorphous silicon layer (item 4a in Fig. 1, described in the specification on page 6 line 7) directly on a first metal layer (item 3a in fig.1, described in specification on page 6 line 3), which in turn overlays the high k gate insulator layer (item 2a in fig. 1, described in the specification on page 5 line 15) ; patterning to form an amorphous silicon shape (item 4b in fig 2, described in specification on page 6 line 20) and an underlying metal gate structure(item 3b in fig. 2, described in the specification on page 6 line 20). After formation of silicon nitride/silicon oxide composite insulator spacers (items 7 and 8 in fig.4, and described in the specification on page 7 line 16 to page 8 line 3) on the sides of the amorphous silicon shape and the metal gate structure a second metal layer (item 10a in fig 6, described in specification on page 8 line 14) is deposited followed by an anneal procedure resulting in a metal silicide region (item 10c in fig. 7 and in the specification on page 9 line 13) formed on the underlying metal gate structure via total consumption of the second metal layer and via total consumption of the amorphous silicon region. Non-reacted portions of the second metal layer ((items 10a, in fig. 7, described in specification on page 9 line 13) residing on the sides of the composite insulator spacers are selectively removed. The essence of Independent Claim 16 is the deposition of the amorphous silicon layer directly on an underlying first metal layer and after patterning of

the amorphous silicon layer and the first metal layer to form a gate structure, a second metal layer is deposited directly on the amorphous silicon shape with a subsequent anneal procedure resulting in the formation of a metal silicide region directly on an underlying first metal gate structure, again via total consumption of the second metal layer and of an amorphous silicon shape and without the use of a stop layer located between the amorphous silicon shape and the underlying metal gate structure.

Dependent Claims 17, 18, and 19, described in the Specification on page 5, lines 12 - 15, describe an N channel, P channel or complimentary (CMOS) MOSFET device to which this process is applied to.

Dependent Claim 20 described in the Specification on page 5 line 17 to page 6, line 6, and shown schematically in Fig 1, describe a group of high k gate insulator layers from which the gate insulator layer can be chosen from.

Dependent Claim 21, described in the Specification on page 5 line 17 to page 6, line 6, and shown schematically in Fig 1, describe the thickness and dielectric constant of the high k gate insulator layer.

Dependent Claim 22, described in the Specification on page 6 line 3 to page 6 line 6, and shown schematically in Fig. 1, describe the group of metals from which the first metal layer can be chosen from in addition to describing the thickness range of the first metal as well as the mode

of deposition

Dependent Claim 23, described in the Specification on page 6 line 6 to page 6 line 11, and shown schematically in Fig. 1, describe the amorphous silicon layer, the thickness and mode of deposition of the amorphous silicon layer.

Dependent Claim 24, described in the Specification on page 6 line to page 6 line 21, as well as shown schematically in Fig. 2, describe the definition mode and reactant gas used to define the amorphous silicon shape and underlying metal gate shape.

Dependent Claims 25 and 26, described in the Specification on page 7 line 14 to page 8 line 3, as well as schematically shown in Fig. 4, describe the deposition modes as well as the thickness range for the silicon oxide and silicon nitride layers to be used for a composite insulator layer.

Dependent Claim 27, described in the Specification on page 8 line 14 to page 8 line 17, as well as schematically in Fig. 6, describe a group of metals that the second metal layer can be chosen from, while also describing the thickness and mode of deposition of the second metal layer.

Dependent Claim 28, the anneal procedure and conditions used to form metal silicide are described in the Specification on page 8 line 18 to page 9 line 12, as well as in Fig. Fig. 7.

Dependent Claims 29 and 30 have been previously cancelled.

Dependent Claim 31, described in the Specification on page 9 line 13 to page 9 line 21, and schematically in Fig. 8, describe the selective removal of non-reacted portions of the second metal from the surfaces of the insulator spacers.

GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

The rejection of Claims 1-6, 9-12, and 14 under 35 U.S.C. 103(a) as being unpatentable over Bai et al (US 5,818,092), in view of Deshpande et al (US 6,512,266 B1).

The rejection of Claim 8 under 35 U.S.C. 103(a) as being unpatentable over Bai et al (US 5,818,092), taken with Deshpande et al (US 6,512,266 B1) and in further view of Wu (US 6,130,135).

The rejection of Claim 15 under USC 103(a) as being unpatentable over Bai et al (US 5,818,092), taken with Deshpande et al (US 6,512,266 B1) and in further view of Tsai et al (US 2002/0192932) and Wieczorek et al (US 6,274,511).

The rejection of Claims 16- 21, and 24- 28 under USC 103(a) as being unpatentable over Bai et al (US 5,818,092), taken with Deshpande et al (US 6,512,266 B1) and in further view of Wieczorek et al (US 6,274,511).

The rejection of Claim 23 under USC 103(a) as being unpatentable over Bai et al (US 5,818,092), taken with Deshpande et al (US 6,512,266 B1) and Wieczorek et al (US 6,274,511).

The rejection of Claim 31 as being unpatentable over Bai et al (US 5,818,092), taken with Deshpande et al (US 6,512,266) and Wieczorek et al (US 6,274,511)Tsai et al (US 2002/0192932).

The rejection of Claims 1- 4, 6-7, and 9, under USC 103(a) as being unpatentable over Chau et al (US 5,625,217) and in view of Nguyen et al (US 6,084,279).

The rejection of Claims 5 and 10 under USC 103(a) as being unpatentable over Chau et al (US 5,625,217) and in view of Nguyen et over Chau et al (US 5,625,217) and taken with Nguyen et al and in view of Deshpande et al.

The rejection of Claims 16 - 22, 24 - 26 and 28 under USC 103(a) as being unpatentable over Chau et al (US 5,625,217) taken with Nguyen and Deshpande and in further view of Wieczorek.

The rejection of Claim 23, under USC 103(a) as being unpatentable over Chau et al (US 5,625,217) taken with Nguyen, Deshpande and Wieczorek and in further view of Wu.

The rejection of Claim 31 under USC 103(a) as being unpatentable over Chau et al (US 5,625,217) taken with Nguyen, Deshpande and Wieczorek and in further view of Tsai

ARGUMENT

Rejection of Claims 1-6, 9-12, and 14 under 35 U.S.C. 103(a) as being unpatentable over Bai et al (US 5,818,092), in view of Deshpande et al (US 6,512,266 B1).

A key feature of applicant's process invention is the formation of a metal silicide region, such as region 10c in Fig. 7, via total consumption of amorphous shape 4b, Fig 6. This will result in the desirable situation in which metal silicide region 10c resides directly on underlying conductive shape 3b, without any other layers between. This will, in contrast to having interceding materials between, allow the lowest gate structure resistance. It is difficult to form metal silicide directly on an underlying conductive gate shape via total consumption of an amorphous silicon shape and therefore during silicide formation others including Bai et al use a layer between the metal and conductive layers to avoid the silicide process from unwanted attack of the underlying conductive gate structure. It is clear that Bai et al do use this protective layer, layer 206 in Fig. 2a- 2c, and this layer unlike applicant's invention remains as a component of their final composite conductive gate structure. Applicant clearly in independent Claim 1 states no interceding steps between deposition of the conductive layer and the amorphous silicon thus preluding the use of a costly and complex stop layer deposition. In addition applicant's Claim 1 states the metal silicide region is formed directly on on underlying conductive gate structure. This is surely significant process differences when compared to the Bai et al prior art. However Examiner in final office action dated 04/03/2007, still claims the Bai prior art does show formation of a metal silicide layer directly on an underlying conductive shape, however the

text and drawings in the Bai prior art show different, that is the use of stop layer 206.

The feature of the Deshpande et al prior art noted by Examiner is only to show a composite insulator spacer on the sides of the conductive gate structure, nothing to give evidence of applicant's unique process sequence. Therefore is it believed that there is no evidence that the Bai et al and Deshpande et al prior art can be combined to result in applicant's process in which a metal silicide region is formed directly on an underlying conductive gate structure without the use of a stop layer residing on the top surface of the conductive gate structure.

Rejection of Claim 8 under 35 U.S.C. 103(a) as being unpatentable over Bai et al (US 5,818,092), taken with Deshpande et al (US 6,512,266 B1) and in further view of Wu (US 6,130,135).

Examiner cites the Wu prior art in which deposition of an amorphous silicon layer is shown. However applicant's dependent Claim 8 describing a amorphous silicon layer is shown as a reference to independent Claim 1 in which an amorphous silicon layer is used as a component during a silicide formation. Therefore the combination of the above prior art does not present applicant's invention where a metal silicide region is formed directly on an underlying conductive gate structure without the use of a stop layer used on the top surface of the underlying conductive gate shape.

Rejection of Claim 15 under USC 103(a) as being unpatentable over Bai et al (US 5,818,092), taken with Deshpande et al (US 6,512,266 B1) and in further view of Tsai et al

(US 2002/0192932) and Wieczorek et al (US 6,274,511).

This rejection is based on the Wieczorek et al invention in which non-reacted metal is removed from the surfaces of the composite insulator spacers. Applicant's dependent Claim 15 is only used to reference applicant's novel independent Claim 1, and therefore it is again believed that no combination of the above prior art can result in applicant's process.

Rejection of Claims 16- 21, and 24- 28 under USC 103(a) as being unpatentable over Bai et al (US 5,818,092), taken with Desphpande et al (US 6,512,266 B1) and in further view of Wieczorek et al (US 6,274,511).

As previously stated when reviewing independent Claim 1, applicant clearly describes the formation of a metal silicide region directly on an conductive gate shape via total consumption of metal and amorphous silicon components. Examiner again refers to the Bai invention in which (Fig. 2a-2c) a stop layer 206 is used between the overlying amorphous silicon layer 208 and an underlying gate structure 204. Applicant's key feature is a process sequence that does no employ a stop layer such as Bai's layer 206. It is advantageous to be able to form metal silicide directly on the underlying gate structure in terms of cost and process complexity, thus is applicant's process were known or disclosed it would surely be employed. There is no evidence of this in any of, or in any combination of the above prior art.

Rejection of Claim 23 under USC 103(a) as being unpatentable over Bai et al (US 5,818,092), taken with Deshpande et al (US 6,512,266 B1) and Wieczorek et al (US 6,274,511).

Examiner claims the combination of the above prior can result in applicant's process citing the Wu prior art in which deposition of an amorphous silicon layer is shown. However applicant's dependent Claim 23 describing an amorphous silicon layer is shown as a reference to independent Claim 16 in which an amorphous silicon layer is used as a component during a silicide formation. Therefore the combination of the above prior art does not present applicant's invention where a metal silicide region is formed directly on an underlying conductive gate structure without the use of a stop layer used on the top surface of the underlying conductive gate shape.

Rejection of Claim 31 as being unpatentable over Bai et al (US 5,818,092), taken with Deshpande et al (US 6,512,266) and Wieczorek et al (US 6,274,511)Tsai et al (US 2002/0192932).

This rejection is based on the Tsai et al invention in which non-reacted metal is removed from the surfaces of the composite insulator spacers. Applicant's dependent Claim 31 is only used to reference applicant's novel independent Claim 16, which no combination of the Bai et, Deshpande et al, and Wieczoreck et al can result in applicants invention and the inclusion of the Tsai prior art, just describing removal of non-reacted metal, still does not result in a combination of prior art suggesting applicant's process.

Rejection of Claims 1- 4, 6-7, and 9, under USC 103(a) as being unpatentable over Chau et al (US 5,625,217) and in view of Nguyen et al (US 6,084,279).

As clearly described in independent Claim 1 of applicant's process invention the desired metal silicide region is formed directly on the underlying conductive gate structure via total consumption of the amorphous silicon shape. The Chau et al prior, as shown in Fig. 4g, clearly show metal silicide layer 524 formed via only via partial consumption of silicon layer 512. The Nguyen et al prior art only describe fabrication of a gate structure never claiming metal silicide formation on an underlying gate structure achieved via total consumption of the components, a metal layer an amorphous silicon layer. Therefore there is no evidence that the combination of the Chau and Nguyen art could lead one to applicant's process.

Rejection of Claims 5 and 10 under USC 103(a) as being unpatentable over Chau et al (US 5,625,217) and in view of Nguyen et over Chau et al (US 5,625,217) and taken with Nguyen et al and in view of Desphande et al.

The above Claims 5 and 10, are used to describe specific semiconductor process sequences and are used to reference applicant's unique independent Claims 1 and 16, in which again a metal silicide region is formed directly on an underlying conductive gate structure via total consumption of an amorphous silicon shape and an overlying metal layer.

Rejection of Claims 16 - 22, 24 - 26 and 28 under USC 103(a) as being unpatentable over Chau et al (US 5,625,217) taken with Nguyen and Desphande and in further view of Wieczorek.

Applicant's independent Claim 16 features a metal silicide region formed directly on an underlying conductive gate structure via total consumption of an amorphous silicon shape and of an overlying metal layer. The combination of the above prior art still can not be used to describe applicant's independent Claim 16.

Rejection of Claim 23, under USC 103(a) as being unpatentable over Chau et al (US 5,625,217) taken with Nguyen, Desphande and Wieczorek and in further view of Wu.

Applicant's dependent Claim 23 describing an amorphous silicon layer is shown as a reference to independent Claim 16 in which an amorphous silicon layer is used as a component during a silicide formation. The above prior art describing an amorphous silicon layer still do not combine to describe applicant's invention where a metal silicide region is formed directly on an underlying conductive gate structure without the use of a stop layer used on the top surface of the underlying conductive gate shape

The rejection of Claim 31 under USC 103(a) as being unpatentable over Chau et al (US 5,625,217) taken with Nguyen, Desphande and Wieczorek and in further view of Tsai

This rejection is based on the Tsai et al invention in which non-reacted metal is removed from the surfaces of the composite insulator spacers. Applicant's dependent Claim 31 is only used to reference applicant's novel independent Claim 16. No combination of the Chau et al, Nguyen, Deshpande et al, and Wieczoreck et al can result in applicants invention and the

inclusion of the Tsai prior art, just describing removal of non-reacted metal, still does not result in combination of prior art suggesting applicant's process.

SUMMARY

It is believed that Claims 1 - 12, 14 - 28 and 31 distinguish patentable from the references and should be allowed.

Applicant requests that the Board of Appeals reverse the final rejection of Claims 1-6, 9-12, and 14 under 35 U.S.C. 103(a) as being unpatentable over Bai et al (US 5,818,092), in view of Deshpande et al (US 6,512,266 B1).

Applicant further requests that the Board of Appeals reverse the final rejection of Claim 8 under 35 U.S.C. 103(a) as being unpatentable over Bai et al (US 5,818,092), taken with Deshpande et al (US 6,512,266 B1) and in further view of Wu (US 6,130,135).

Applicant further requests that the Board of Appeals reverse the final rejection of Claim 15 under USC 103(a) as being unpatentable over Bai et al (US 5,818,092), taken with Deshpande et al (US 6,512,266 B1) and in further view of Tsai et al (US 2002/0192932) and Wieczorek et al (US 6,274,511).

Applicant further requests that the Board of Appeals reverse the final rejection of Rejection of Claims 16- 21, and 24- 28 under USC 103(a) as being unpatentable over Bai et al (US 5,818,092), taken with Deshpande et al (US 6,512,266 B1) and in further view of Wieczorek et al (US 6,274,511).

Applicant further requests that the Board of Appeals reverse the final rejection of of Claim 23 under USC 103(a) as being unpatentable over Bai et al (US 5,818,092), taken with Deshpande et al (US 6,512,266 B1) and Wieczorek et al (US 6,274,511).

Applicant further requests that the Board of Appeals reverse the final rejection of Claim 31 as being unpatentable over Bai et al (US 5,818,092), taken with Deshpande et al (US 6,512,266) and Wieczorek et al (US 6,274,511)Tsai et al (US 2002/0192932).

Applicant further requests that the Board of Appeals reverse the final rejection of Claims 1- 4, 6-7, and 9, under USC 103(a) as being unpatentable over Chau et al (US 5,625,217) and in view of Nguyen et al (US 6,084,279).

Applicant further requests that the Board of Appeals reverse the final rejection of Claims 5 and 10 under USC 103(a) as being unpatentable over Chau et al (US 5,625,217) and in view of Nguyen et over Chau et al (US 5,625,217) and taken with Nguyen et al and in view of Deshpande et al.

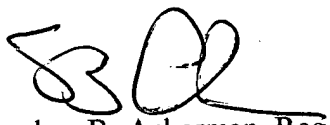
Applicant further requests that the Board of Appeals reverse the final rejection of Claims 16 - 22, 24 - 26 and 28 under USC 103(a) as being unpatentable over Chau et al (US 5,625,217) taken with Nguyen and Deshpande and in further view of Wieczorek.

Applicant further requests that the Board of Appeals reverse the final rejection of Claim 23, under USC 103(a) as being unpatentable over Chau et al (US 5,625,217) taken with Nguyen, Deshpande and Wieczorek and in further view of Wu.

Applicant further requests that the Board of Appeals reverse the final rejection of Claim 31 under USC 103(a) as being unpatentable over Chau et al (US 5,625,217) taken with Nguyen, Deshpande and Wieczorek and in further view of Tsai

Claims 13, 29 and 30 have been cancelled.

Respectfully submitted,



Stephen B. Ackerman, Reg. No. 37,761

CLAIMS APPENDIX

Listing of Claims:

Claim 1 (Previously Presented) A method of forming a metal oxide semiconductor field effect transistor (MOSFET) device on a semiconductor substrate comprising the steps of:

forming a gate insulator layer on said semiconductor substrate;

forming a conductive layer on said gate insulator layer, wherein said conductive layer is formed of a single material;

without inclusion of any interceding steps immediately forming an amorphous silicon layer, wherein said amorphous silicon layer is formed of a single material, directly on said conductive layer;

defining a conductive gate structure and an overlying amorphous silicon shape, on said gate insulator layer;

removing portion of said gate insulator layer not covered by said conductive gate structure;

forming a first doped region in an area of said semiconductor substrate not covered by said conductive gate structure;

forming composite insulator spacers on the sides of said conductive gate structure and on the sides of said amorphous silicon shape;

forming a second doped region in an area of said semiconductor substrate not covered by said conductive gate structure, or by said composite insulator spacers;

forming a metal layer, wherein said metal layer is formed of a single material;

performing an anneal procedure to form first metal silicide regions from an overlying first portion of said metal layer and from a top portion of said second doped region, and to form a second metal silicide region directly on said conductive gate structure from an overlying second portion of said metal layer via total consumption of said amorphous silicon shape, while third portions of said metal layer located on said composite insulator spacers remain unreacted; and

removing unreacted portions of said metal layer located on said composite insulator spacers.

Claim 2. (Original) The method of claim 1, wherein said MOSFET device is an N channel MOSFET device.

Claim 3. (Original) The method of claim 1, wherein said MOSFET device is a P channel MOSFET device.

Claim 4. (Original) The method of claim 1, wherein said MOSFET device is a complimentary metal oxide semiconductor (CMOS) device, comprised with both N channel and P channel MOSFET devices.

Claim 5. (Original) The method of claim 1, wherein said gate insulator layer is a high dielectric constant (high k) layer selected from a group consisting of silicon nitride, tantalum oxide, silicon oxynitride, zirconium oxide, hafnium oxide, aluminum oxide, all with a dielectric constant greater than 4.

Claim 6. (Original) The method of claim 1, wherein the thickness of said gate insulator layer is between about 15 to 500 Angstroms.

Claim 7. (Previously presented) The method of claim 1, wherein said conductive layer, formed of a single material, is a refractory metal such as tungsten or molybdenum, obtained via physical vapor deposition procedures at a thickness between about 800 to 2000 Angstroms.

Claim 8. (Previously presented) The method of claim 1, wherein said amorphous silicon layer, formed of a single material, is obtained at a thickness between about 200 to 1000 Angstroms, via a low pressure chemical vapor deposition (LPCVD), or via a plasma enhanced chemical vapor deposition (PECVD) procedure.

Claim 9. (Previously presented) The method of claim 1, wherein said conductive gate structure and said overlying amorphous silicon shape are defined via an anisotropic reactive ion etch procedure using Cl_2 as an etchant for said amorphous silicon layer and for said conductive layer.

Claim 10. (Original) The method of claim 1, wherein said composite insulator spacers are comprised of an underlying silicon oxide shape at a thickness between about 50 to 250 Angstroms, and an overlying silicon nitride shape at a thickness between about 300 to 1000 Angstroms.

Claim11. (Original) The method of claim 1, wherein said metal layer is selected from a group consisting of titanium, cobalt, nickel, zirconium, tantalum, or nickel - platinum, obtained via physical vapor deposition procedures at a thickness between about 50 to 500 Angstroms..

Claim 12. (Original) The method of claim 1, wherein said anneal procedure used to form metal silicide regions is a rapid thermal anneal procedure performed in an inert ambient at a temperature between about 450 to 900° C, for a time between about 30 to 400 sec.

Claim 13. (Cancelled)

Claim 14. (Previously presented) The method of claim 1, wherein second metal silicide region located directly on said conductive gate structure, is formed consuming all of said amorphous silicon shape.

Claim 15. (Original) The method of claim 1, wherein unreacted portions of said metal layer are removed via a wet procedure using a solution comprised of HCl - H_2O_2 - NH_4OH - H_2SO_4.

Claim 16. (Previously Presented) A method of forming a MOSFET device on a semiconductor substrate featuring a metal silicide region on a metal gate structure, comprising the steps of:

forming a high dielectric constant (high k), gate insulator layer on said semiconductor substrate;

forming a first metal layer on said high k gate insulator layer wherein said first metal layer is formed of a single material;

without performing any interceding steps immediately forming an undoped amorphous silicon layer on said first metal layer, wherein said amorphous silicon layer is formed of a single material;

performing a first anisotropic reactive ion etch (RIE) procedure to define a metal gate structure and an overlying amorphous silicon shape directly on said high k gate insulator layer;

removing portion of said high k gate insulator layer not covered by said metal gate structure;

forming a lightly doped source/drain region in an area of said semiconductor substrate not covered by said metal gate structure;

forming a silicon oxide layer;

forming a silicon nitride layer;

performing a second anisotropic RIE procedure to form composite insulator spacers comprised of an overlying silicon nitride shape and an underlying silicon oxide shape, on the sides of said metal gate structure and on the sides of said amorphous silicon shape;

forming a heavily doped source/drain region in an area of said semiconductor substrate not covered by said metal gate structure, or by said composite insulator spacers;

forming a second metal layer ,wherein said second metal layer is formed of a single material;

performing a first anneal procedure to form first metal silicide regions from an overlying first portion of said second metal layer and from a top portion of said heavily doped source/drain region, and to form a second metal silicide region from an overlying second portion of said metal layer and from said amorphous silicon shape completely consuming said amorphous silicon shape, while a third portion of said second metal layer located on said composite insulator spacers remain unreacted;

removing unreacted third portion of said second metal layer; and

performing a second anneal procedure.

Claim17. (Original) The method of claim 16, wherein said MOSFET device is an N channel MOSFET device.

Claim 18. (Original) The method of claim 16, wherein said MOSFET device is a P channel MOSFET device.

Claim 19. (Original) The method of claim 16, wherein said MOSFET device is a complimentary metal oxide semiconductor (CMOS) device, comprised with both N channel and P channel MOSFET devices.

Claim 20. (Original) The method of claim 16, wherein said high k gate insulator layer is selected from a group consisting of silicon nitride, tantalum oxide, silicon oxynitride, zirconium oxide, hafnium oxide, aluminum oxide.

Claim 21. (Original) The method of claim 16, wherein said high k gate insulator layer is comprised with a dielectric constant greater than 4, and at a thickness between about 15 to 150 Angstroms.

Claim 22. (Original) The method of claim 16, wherein said first metal layer is a refractory metal such as tungsten or molybdenum, obtained via physical vapor deposition procedures at a thickness between about 800 to 2000 Angstroms.

Claim 23. (Original) The method of claim 16, wherein said amorphous silicon layer is obtained at a thickness between about 200 to 1000 Angstroms, via a low pressure chemical vapor deposition (LPCVD), or via a plasma enhanced chemical vapor deposition (PECVD) procedure.

Claim 24. (Original) The method of claim 16, wherein said first anisotropic RIE procedure used to define said metal gate structure and said overlying amorphous silicon shape is performed using Cl_2 as an etchant.

Claim 25. (Original) The method of claim 16, wherein said silicon oxide layer is obtained via LPCVD or via PECVD procedures at a thickness between about 50 to 250 Angstroms

Claim 26. (Original) The method of claim 16, wherein said silicon nitride layer is obtained via LPCVD or via PECVD procedures a thickness between about 300 to 1000 Angstroms.

Claim 27. (Original) The method of claim 16, wherein said second metal layer is selected from a group consisting of titanium, cobalt, nickel, zirconium, tantalum, or nickel - platinum, obtained via physical vapor deposition procedures at a thickness between about 50 to 500 Angstroms.

Claim 28. (Original) The method of claim 16, wherein said first anneal procedure used to form metal silicide regions is a rapid thermal anneal (RTA) procedure performed in an inert ambient at a temperature between about 450 to 900° C, for a time between about 30 to 400 sec.

Claim 29. (Cancelled)

Claim 30. (Cancelled)

Claim 31. (Original) The method of claim 16 wherein said unreacted portion of said third metal layer is removed via a wet procedure using a solution comprised of HCl - H_2O_2 - NH_4OH - H_2SO_4.

EVIDENCE APPENDIX

None

RELATED PROCEEDINGS APPENDIX

None